Tco_Xmt_Max/Min

Xmt2FPGA_BrdDly_Max/Min

FPGA2Rcv_BrdDly_Max/Min

Tsu_Rcv
Thd_Rcv

D Q

5   6   Data_In

D Q   D Q   Data_Out   7   8   D Q

External
Device A
Xmt

PLL

Device B
FPGA

External
Device C
Rcv

2   FPGA_Clk   3   4

ExtClk

Board
Clock
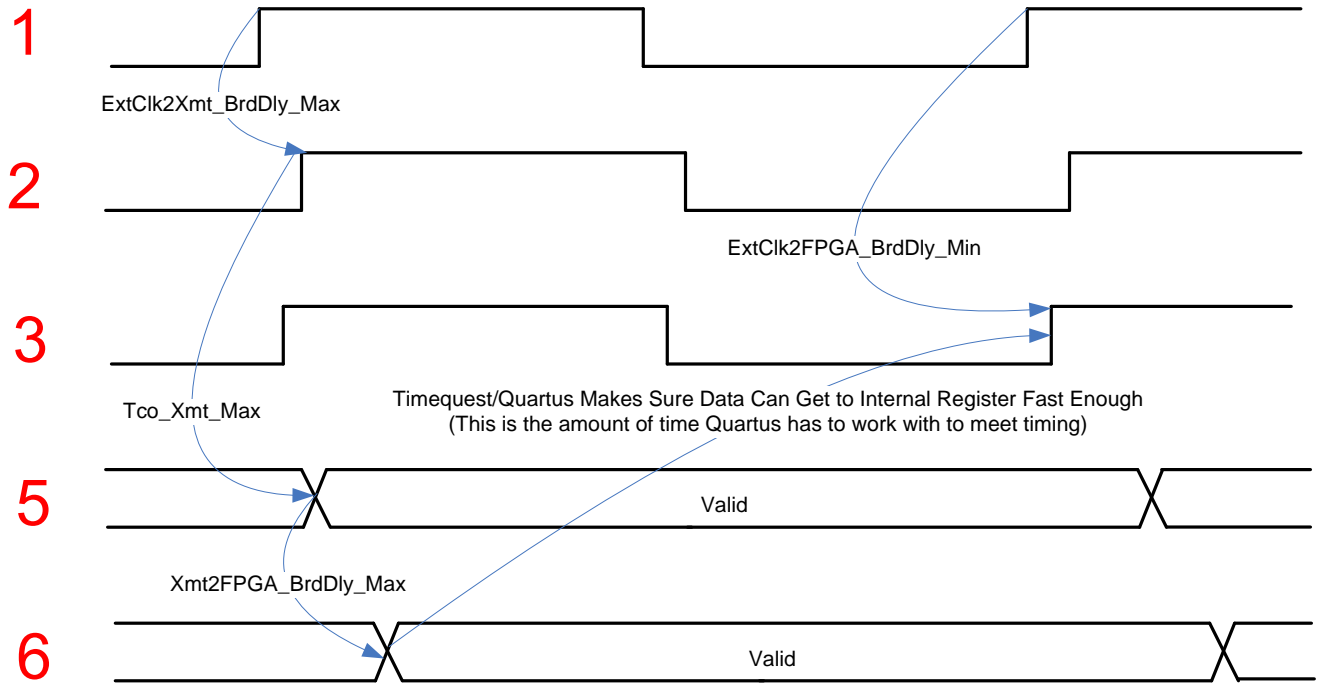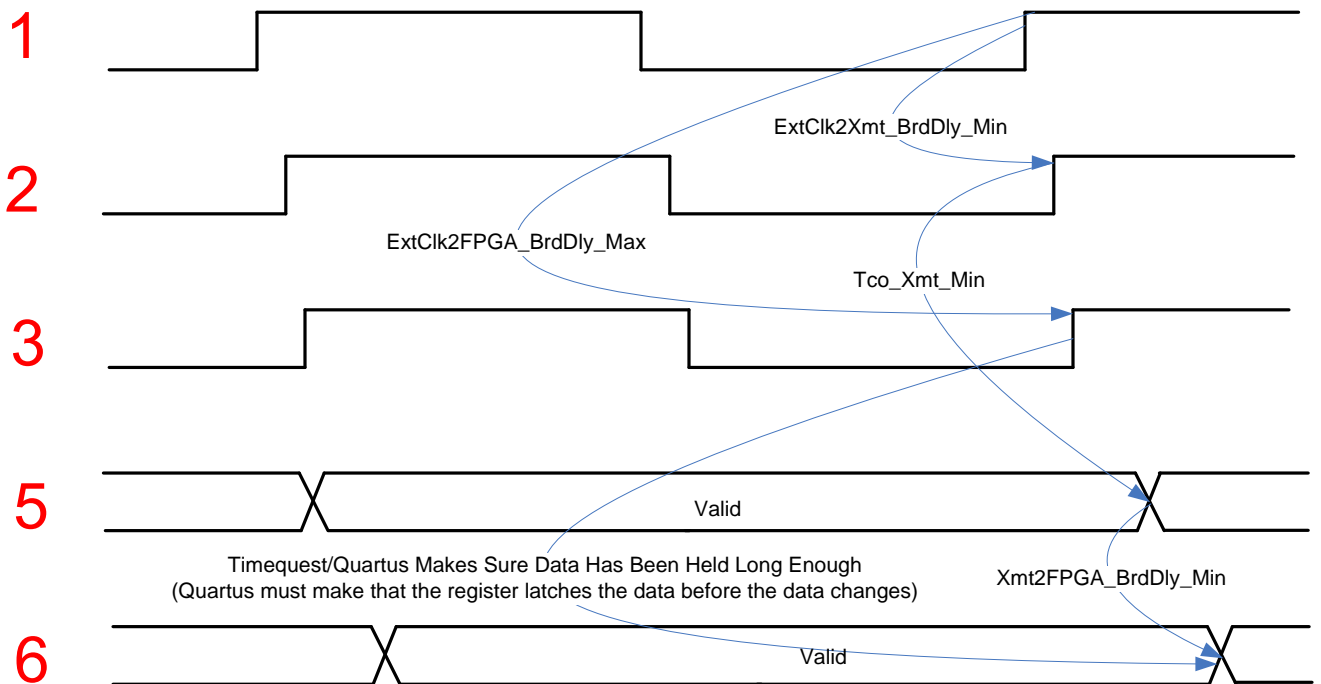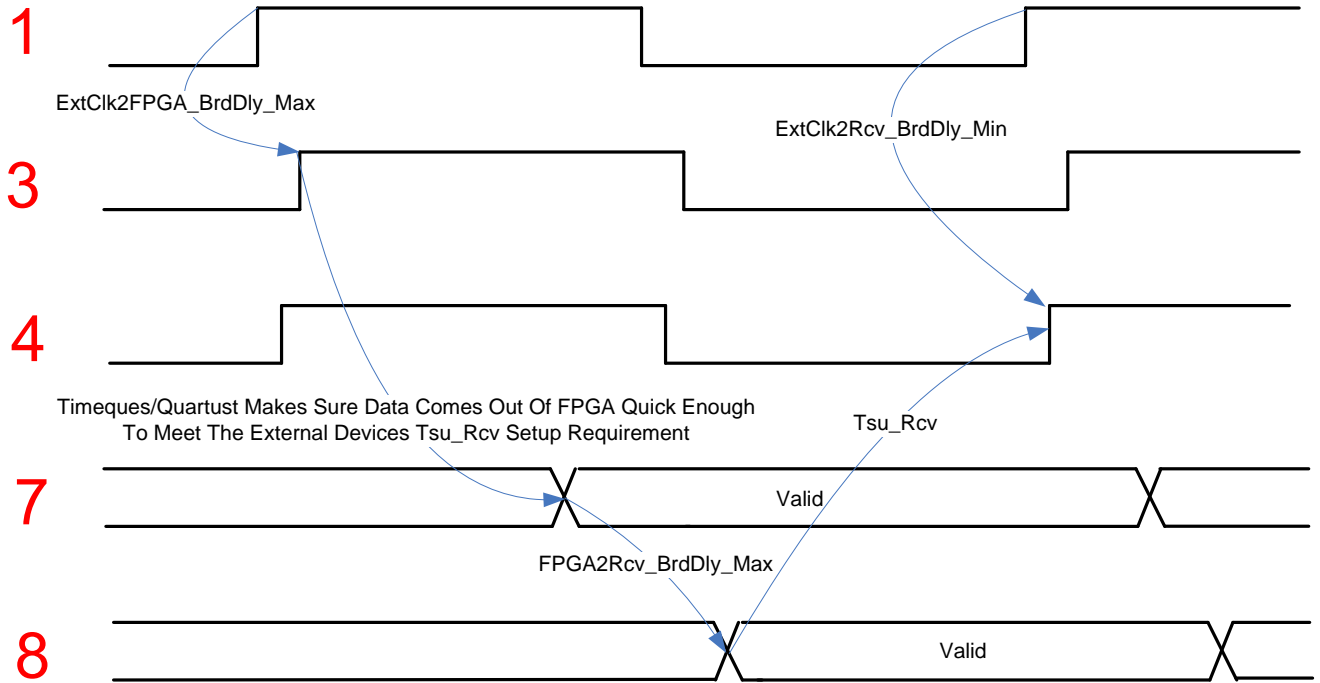Generation

1

ExtClk2Xmt_BrdDly_Max/Min

ExtClk2FPGA_BrdDly_Max/Min

ExtClk2Rcv_BrdDly_Max/Min

Timequest/Quartus Setup Analysis From External Xmt Device to FPGA
Use Slow Timing Models for Setup Analysis

1

ExtClk2Xmt_BrdDly_Max

2

ExtClk2FPGA_BrdDly_Min

3

Tco_Xmt_Max

Timequest/Quartus Makes Sure Data Can Get to Internal Register Fast Enough
(This is the amount of time Quartus has to work with to meet timing)

5   Valid

Xmt2FPGA_BrdDly_Max

6   Valid

Timeques/Quartust Hold Analysis From External Xmt Device to FPGA
Use Fast Timing Models for Hold Analysis

1

ExtClk2Xmt_BrdDly_Min

2

ExtClk2FPGA_BrdDly_Max

Tco_Xmt_Min

3

5   Valid

Timequest/Quartus Makes Sure Data Has Been Held Long Enough
(Quartus must make that the register latches the data before the data changes)

Xmt2FPGA_BrdDly_Min

6   Valid

Timequest Setup Analysis From FPGA to External Rcv Device
Use Slow Timing Models for Setup Analysis

1

ExtClk2FPGA_BrdDly_Max

ExtClk2Rcv_BrdDly_Min

3

4

Timeques/Quartust Makes Sure Data Comes Out Of FPGA Quick Enough
To Meet The External Devices Tsu_Rcv Setup Requirement

Tsu_Rcv

7

Valid

FPGA2Rcv_BrdDly_Max

8

Valid

Timequest/Quartus Hold Analysis From FPGA to External Rcv Device
Use Fast Timing Models for Hold Analysis

1

ExtClk2FPGA_BrdDly_Min

3

ExtClk2Rcv_BrdDly_Max

4

Timequest/Quartus Makes Sure the FPGA Data Has Enough Delay To Meet
The External Device's Thd_Rcv Hold Requirement

Thd_Rcv

7

Valid

FPGA2Rcv_BrdDly_Min

8

Valid